REMARKS

Applicant respectfully requests allowance of the subject application.

Claims 1, 11, 19, 35, 42, 45, 51, 56 and 63-64 are amended.

Claims 4, 12, 20, 37, 47 and 68 are cancelled.

Claims 1-3, 5-11, 13-19, 21-36, 38-46 and 48-67 are pending.

In view of the following remarks, Applicant respectfully requests that the rejections be withdrawn and the application be forwarded along to issuance

§§ 102(b) Rejection

Claims 1-9, 11-17, 19-22, 24-33 and 35-68 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,560,676 to Nishimoto et al. (hereinafter "Nishimoto"). The Applicant respectfully disagrees. First, it should be noted that Nishimoto was not published more than one year before the filing date of the subject Application, and therefore is not 102(b) art. Therefore, the Applicant will assume that the Office instead meant 102(e).

Claim 1 has been amended, and as amended (portions of the amendment appear in bold/italics below) recites a method comprising:

- issuing a cache residency test instruction for a set of data; and
- determining with a processor unit using the issued cache residency test instruction if the set of data resides in a cache memory that is communicatively coupled to the processor unit;
- ***establishing a relative amount of time to access the set of data by the processor unit;*** and
- communicating a result of the determining to software being executed on the processor unit.

Support for the amendment may be found throughout the specification and drawings as filed, such as in originally filed Claim 4.

Claim 19 has been amended, and as amended (portions of the amendment appear in bold/italics below) recites a method comprising:

- comparing an address of a set data with at least one other address in a cache memory, wherein the cache memory includes a plurality of levels and is communicatively coupled to a processor unit;
- providing an indication to the processor unit, based on the comparing whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included;
- ***establishing a relative amount of time to access the set of data, by the processor unit, based on which level of the plurality of levels the address is included;*** and
- communicating the indication, by the processor unit, to software being executed on the processor unit.

Support for the amendment may be found throughout the specification and drawings as filed, such as in originally filed Claim 20.

Claim 24, as originally filed, recites a method comprising:

- supplying an address for a set of data to a comparison unit from a processor unit;
- comparing with the comparison unit the address for the set of data with an address in the cache memory;
- indicating to the processor unit from the comparison unit based on the comparing whether the address of the set of data is included in the cache memory;
- establishing based on the indicating of whether the address of the set of data is included in the cache memory a relative amount of time to access the set of data by the processor unit; and
- communicating the established relative amount of time to software being executed by the processor unit.

Claim 35 has been amended, and as amended (portions of the amendment appear in bold/italics below) recites for use on a processor unit that is communicatively coupled to a cache memory, a cache residency test instruction, executable on the processor unit, which when executed on the processor unit configures the processor unit to performs acts comprising:

- querying whether a set of data resides in the cache memory;
- receiving an indication from the querying of whether the set of data resides in the cache memory;
- ***establishing a relative amount of time to access the set of data by the processor unit, wherein the establishing is based on the indication which indicates whether the set of data resides in the cache memory;*** and
- communicating the indication ***and the relative amount of time*** to software being executed on the processor unit.

Support for the amendment may be found throughout the specification and drawings as filed, such as in originally filed Claim 37.

Claim 45 has been amended, and as amended (portions of the amendment appear in bold/italics below) recites a system comprising:

- a cache memory; and
- a processor unit communicatively coupled to the cache memory, wherein the processor unit includes a cache residency test instruction that, when executed, configures the processor unit:
  - to query whether a set of data resides in the cache memory;
  - to receive an indication from the query of whether the set of data resides in the cache memory;
  - ***to establish a relative amount of time to access the set of data;*** and
  - to communicate the indication ***and the relative amount of time*** to software being executed on the processor unit.

Support for the amendment may be found throughout the specification and drawings as filed, an example of which may be found in originally filed claim 47.

Claim 51 has been amended, and as amended (portions of the amendment appear in bold/italics below) recites a system comprising:

- a processor unit;
- a comparison unit communicatively coupled to the processor unit; and
- a cache memory communicatively coupled to the comparison unit, wherein the comparison unit is configured:
  - to compare an address received from the processor unit with at least one address in the cache memory; and
  - to provide an indication to the processor unit indicating whether the address is included in the cache memory based on the comparison ***such that the processor unit is configured to establish a relative amount of time to access a set of data specified by the address***.

Support for the amendment may be found throughout the specification and drawings as filed.

Claim 56 has been amended, and as amended (portions of the amendment appear in bold/italics below) recites a processor chip comprising:

- a processor unit having a coupling for communicatively coupling the processor unit to a cache memory, wherein:
  - the processor unit includes storage for a cache residency test instruction; and
  - an execution of the cache residency test instruction with the processor unit configures the processor unit to determine if a set of data resides in the cache memory, ***establish a relative amount of time to access the set of data,*** and communicate a result of the determination ***and the relative amount of time*** to software being executed on the processor unit.

Support for the amendment may be found throughout the specification and drawings as filed.

Beginning at page 10 of the subject Application, exemplary execution of a residency instruction is described. An execution of the residency instruction is used to improve the interaction of the processor chip with the cache memory, and more particularly, to improve performance of software being executed on the processor chip. The residency instruction, when executed on the processor chip, is used to determine if a set of data resides in the cache memory. Through execution of the residency instruction, the processor chip may recognize characteristics likely to be encountered when accessing the set of data. For example, characteristics of data access may include whether the set of data resides in the cache memory, and therefore may be accessed with minimal delay, or whether the set of data resides in other portions of the memory, such as RAM, peripheral memory, and the like. Therefore, the processor chip may establish a relative amount of time it will take to access the set of data, without actually accessing the set of data, e.g. reading or writing the set of data. The processor chip may communicate a result of the determination to software being executed on the processor chip such that the software may use the result to plan the next actions to be performed when executing the software. For instance, the software may determine which operation to perform first based on whether a set of data that will be the subject of the operation is available from the cache memory.

The Examiner, in the rejection of Claims 4, 20, 24, 37 and 47, asserts generally that "a relative amount of time to access the set of data by the processor unit is equivalently taught as the implementation of LRU algorithm wherein timing is taken into account for access the requested data. In LRU allocation (e.g. see column 2, lines 24 et seq.; for example, a temporal indicator or time stamp is stored for each cache block when data is written into the cache location; by this

rationale, claim 4 is rejected". *See, e.g., Office Action Dated July 28, 2005, Pages 4, 8-10, 13 and 15.* The portion asserted by the Examiner is excerpted below for the sake of convenience:

> Scalar data such as stack data does not show spatial locality, but shows temporal locality.
>
> In a cache employing a set associative system in which the LRU method is used as a replacement algorithm, when a large array having spatial locality, but not temporal locality is accessed, data having temporal locality such as data in a stack is replaced from the cache, overwriting all data within the cache with the above array. A technique for solving the problem that a block having temporal locality is replaced from the cache by a block having spatial locality, but not temporal locality, as described above, is disclosed, for example, in Japanese Laid-Open Patent Publication No. 7-281957 (1995). According to this technique, when data likely to be used again is first referenced, the LRU function is locked, and the lock is released when the data is used lastly.
>
> In the above LRU lock method, however, the LRU function may not be activated after a process is switched to another process, or cache usage may be reduced. Consider, for example, that the LRU function is locked when a stack is first referenced in a process A,. and then the process A is switched to a process B before the lock is released. In this case, even though the process A has been switched to the process B, the LRU function remains locked. Therefore, the block which has been designated as a replacement target when the LRU function was locked is still a replacement target in the locked column despite switching of the processes. This may cause the locked column of the process B to operate as if the cache were of a direct map type, resulting in a great reduction in cache usage. Thus, the above conventional technique using the LRU function may degrade performance. Use of the LRU lock method disclosed in Japanese Laid-Open Patent Publication No. 7-281957 (1995) may lead to a reduction in cache usage in the multiprocess environment.
>
> The present invention provides a cache memory system

> capable of limiting occurrence of replacement of data having temporal locality due to reference to data having spatial locality, but not temporal locality. In addition it is capable of properly performing the LRU function in a multiprocess environment without employing a special process. *Nishimoto, Col. 2, Lines 23 to 64.*

It should be noted that in neither the above referenced portion, nor elsewhere of Nishimoto, is a "timestamp" or a "temporal indicator" disclosed, taught or suggested. Accordingly, Nishimoto does not disclose, teach or suggest the above recited features and withdrawal of the rejection is respectfully requested.

Claim 11 has been amended, and as amended (portions of the amendment appear in bold/italics below) recites a method comprising:

- querying whether a set of data resides in a cache memory that is communicatively coupled to a processor unit;
- receiving an indication at the processor unit from the querying which indicates whether the set of data resides in the cache memory; and
- communicating the indication to ***an operating system*** being executed on the processor unit.

Support for the amendment may be found throughout the specification and drawings as filed, such as in originally filed claim 12.

Claim 42 has been amended, and as amended (portions of the amendment appear in bold/italics below) recites for use on a processor unit that is communicatively coupled to a comparison unit that is communicatively coupled to a cache memory, a cache residency test instruction, which when executed on the processor unit, configures the comparison unit to perform acts comprising:

- comparing an address received from the processor unit with an address in the cache memory;
- providing an indication to the processor unit based on the comparing

of whether the address is included in the cache memory; and
- communicating the indication to ***an operating system*** being executed by the processor unit.

Support for the amendment may be found throughout the specification and drawings as filed.

Claim 63 has been amended, and as amended (portions of the amendment appear in bold/italics below) recites a computing device comprising:

- a storage device; and
- a processor chip, communicatively coupled to the storage device, and including:
- a cache memory; and
- a processor unit communicatively coupled to the cache memory, wherein the processor unit includes storage for a cache residency test instruction that, when executed by the processor unit, configures the processor unit to determine if a set of data resides in the cache memory and to communicate a result of the determination to ***an operating system*** being executed on the processor chip.

Support for the amendment may be found throughout the specification and drawings as filed, such as at originally filed claim 68.

The Examiner, in the rejection of Claims 3, 12, 21, 62 and 68 asserts that "since the operation of Nishimoto's system is clearly software-based and known to have an operating system and application as being claimed". *See Office Action Dated July 27, 2005, Page 3.* This is not the case. First, Nishimoto does not even include the words "operating system". Therefore, Nishimoto cannot disclose, teach or suggest "communicating the indication to ***an operating system*** being executed on the processor unit" as recited in claims 11 and 42, nor "communicate a result of the determination to ***an operating system*** being executed on the

processor chip" as recited in claim 63. Accordingly, withdrawal of the rejection is respectfully requested.

Each of the dependent claims are allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited with their respective independent claims, are neither shown nor suggested in the references of record, either singly or in combination with one another.

Conclusion

All of the claims are in condition for allowance. Accordingly, Applicant requests a Notice of Allowability be issued forthwith. If the Office's next anticipated action is to be anything other than issuance of a Notice of Allowability, Applicant respectfully requests a telephone call for the purpose of scheduling an interview.

Respectfully Submitted,

Dated: 10/28/5

By: _____

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